Claims

What is claimed is:

1. A method for implementing high frequency return current paths utilizing decoupling capacitors within electronic packages comprising the steps of:

receiving electronic package physical design data for identifying a design layout;

utilizing said identified design layout for identifying a respective number of signal vias and a respective number of return current paths for a plurality of cells in a grid of a set cell size within said identified design layout;

calculating ratio of signal vias to return current paths for each of said plurality of cells;

identifying each cell having said calculated ratio greater than a target ratio; and

selectively adding one or more decoupling capacitors within each said identified cell for providing high frequency return current paths.

2. A method for implementing high frequency return current paths within electronic packages as recited in claim 1 wherein the step of receiving electronic package physical design data for identifying said board layout includes the steps of receiving plane stack-up data for identifying reference voltages residing on multiple planes and for creating pairs of reference voltages to be analyzed.

3. A method for implementing high frequency return current paths within electronic packages as recited in claim 1 wherein the step of receiving electronic package physical design data for identifying said board layout includes the step of receiving a board file for identifying locations of high speed nets, locations of plane change vias, and board dimensions.

4. A method for implementing high frequency return current paths within electronic packages as recited in claim 1 includes the step of receiving a user selected value for said target ratio; said target ratio defining a maximum desired ratio of signal vias to return current paths.

5. A method for implementing high frequency return current paths within electronic packages as recited in claim 1 includes the step of receiving a user selected grid dimensions input defining said set cell size.

6. A method for implementing high frequency return current paths within electronic packages as recited in claim 1 wherein the step of selectively adding one or more decoupling capacitors within each said identified cell for providing high frequency return current paths includes the step of identifying nets referenced to at least one reference voltage within each said identified cell.

7. A method for implementing high frequency return current paths within electronic packages as recited in claim 1 wherein the step of selectively adding one or more decoupling capacitors within each said identified cell for providing high frequency return current paths includes the steps of calculating a capacitance value, a capacitor quantity, and optimal placement for adding said one or more decoupling capacitors within said cell.

8. A method for implementing high frequency return current paths within electronic packages as recited in claim 1 wherein the step of selectively adding one or more decoupling capacitors within each said identified cell for providing high frequency return current paths includes the steps of identifying nets referenced to at least one reference voltage within each said identified cell; and connecting said one or more decoupling capacitors between at least one ground plane and at least one plane for said at least one reference voltage within said cell.

9. A method for implementing high frequency return current paths within electronic packages as recited in claim 1 wherein the step of selectively adding one or more decoupling capacitors within each said identified cell for providing high frequency return current paths includes the steps of identifying nets referenced to at least one reference voltage within each said identified cell; and includes the steps of connecting a first decoupling capacitor between a ground plane and one said reference voltage within said cell; and connecting a second decoupling capacitor between said ground plane and another said reference voltage within said cell.

10. A method for implementing high frequency return current paths within electronic packages as recited in claim 9 includes the step of connecting said first decoupling capacitor and said second decoupling capacitor to a plurality of said ground planes.

11. A computer program product for implementing high frequency return current paths within electronic packages in a computer system, said computer program product including instructions executed by the computer system to cause the computer system to perform the steps of:

receiving electronic package physical design data for identifying a design layout;

utilizing said identified design layout for identifying a respective number of signal vias and a respective number of return current paths for a plurality of cells in a grid of a set cell size within said identified design layout;

calculating ratio of signal vias to return current paths for each of said plurality of cells;

identifying each cell having said calculated ratio greater than a target ratio; and

selectively adding one or more decoupling capacitors within each said identified cell for providing high frequency return current paths.

12. A computer program product for implementing high frequency return current paths as recited in claim 11 wherein the step of receiving electronic package physical design data for identifying said board layout includes the steps of receiving plane stack-up data for identifying reference voltages residing on multiple planes and for creating pairs of reference voltages to be analyzed.

13. A computer program product for implementing high frequency return current paths as recited in claim 11 wherein the step of receiving electronic package physical design data for identifying said board layout includes the steps of receiving a board file for identifying locations of high speed nets, locations of plane change vias, and board dimensions.

14. A computer program product for implementing high frequency return current paths as recited in claim 11 includes the steps of receiving a user selected value for said target ratio; said target ratio defining a maximum desired ratio of signal vias to return current paths; and receiving a user selected grid dimensions input defining said set cell size.

15. A computer program product for implementing high frequency return current paths as recited in claim 11 wherein the step of selectively adding one or more decoupling capacitors within each said identified cell for providing high frequency return current paths includes the steps of calculating a capacitance value, a capacitor quantity, and optimal placement for adding said one or more decoupling capacitors within said cell.

16. A computer program product for implementing high frequency return current paths as recited in claim 11 wherein the step of selectively adding one or more decoupling capacitors within each said identified cell for providing high frequency return current paths includes the steps of identifying nets referenced to at least one reference voltage within each said identified cell; and connecting said one or more decoupling capacitors between at least one ground plane and at least one plane for said at least one reference voltage within said cell.

17. Apparatus for implementing high frequency return current paths utilizing decoupling capacitors within electronic packages comprising:

a return path analyzer computer program for receiving electronic package physical design data for identifying a design layout; utilizing said identified design layout for identifying a respective number of signal vias and a respective number of return current paths for a plurality of cells in a grid of a set cell size within said identified design layout; and for calculating ratio of signal vias to return current paths for each of said plurality of cells;

a capacitor calculation tool computer program for identifying each cell having said calculated ratio greater than a target ratio; and for selectively adding one or more decoupling capacitors within each said identified cell for providing high frequency return current paths.

18. Apparatus for implementing high frequency return current paths as recited in claim 17 wherein said electronic package physical design data include plane stack-up data used by said return path analyzer computer program for identifying reference voltages residing on multiple planes and for creating pairs of reference voltages to be analyzed.

19. Apparatus for implementing high frequency return current paths as recited in claim 17 wherein said electronic package physical design data include a board file used by said return path analyzer computer program for identifying locations of high speed nets, locations of plane change vias, and board dimensions.

20. Apparatus for implementing high frequency return current paths as recited in claim 17 wherein said return path analyzer computer program receives a user selected value for said target ratio; said target ratio defining a maximum desired ratio of signal vias to return current paths; and receives a user selected grid dimensions input defining said set cell size.